

Docket No.: 50253-118 (P2287)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Group 2700

MAY 25 2000

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In re Application of

AMIT GUPTA, et al.

Serial No.: 08/868,972

Filed: June 04, 1997

Group Art Unit: 2731

Examiner: Brenda Pham

For: TECHNIQUES FOR IMPROVING VIRTUAL CHANNEL MANAGEMENT AND
MAINTENANCE IN A NETWORK ENVIRONMENT

TRANSMITTAL OF APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Submitted herewith in triplicate is Appellant(s) Appeal Brief in support of the Notice of Appeal filed March 23, 2000. Please charge the Appeal Brief fee of \$300.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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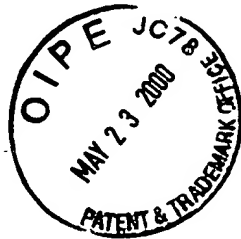
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MAINTENANCE IN A NETWORK ENVIRONMENT

APPEAL BRIEF

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed March 23, 2000 in response to the decision dated December 23, 1999 of the Primary Examiner rejecting claims 1-3 and 6-30 for a second time. These claims had not been amended in the prior response by the Appellants dated November 30, 1999.

REAL PARTY IN INTEREST

The real party in interest is SUN MICROSYSTEMS INC. of Mountain View, California.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences that will affect or be affected by the decision in this case.

STATUS OF CLAIMS

Claims 1-30 remain in the application. Claims 1-3 and 6-30 stand rejected. Claims 4 and 5 stand objected to. The independent claims are 1, 10-11, 17-18, 21 and 23-26.

STATUS OF AMENDMENTS

No amendments have been filed subsequent to the last Office Action.

SUMMARY OF INVENTION

A communications network consists of nodes that are connected by physical links to two or more other nodes or terminals. A user is located at a terminal which is connected by a link to a single node. Each link enters or leaves each node at a physical port of the node. Each node includes many input ports and many output ports, a switch that can be operated to connect any input port to any output port, and a control point to operate the switch. At each node a routing process executes to determine which node is next in a route from the originating node to the destination node and which output ports are associated with the next node. The routing process uses a destination identification specified for information coming in on a particular input port to determine the particular output port to use. The results of the routing process determination is an association, perhaps stored in a look-up table or other data structure. The control point uses the results of the routing process to connect the particular input port to the particular output port.

In some networks, once a series of nodes are used to connect a first user at a first terminal to a second user at a second terminal, the switched connections in each node are maintained until all the information involved in the communications between the first and second user has passed and one or both users terminate the communications session. However, users often utilize only a small fraction of the information carrying capacity of the physical links and switch connections involved. Therefore,

many modern networks share the links and switches to handle many communication sessions concurrently. One method of sharing the hardware links and switches is to communicate with discrete packets, or cells, of information, and to alternate sending packets from different communications sessions over the same physical links and switches. Other methods, such as multiplexing the different communications sessions on different carrier frequencies, are known to those of ordinary skill in the art. Thus instead of devoting a physical connection to each communications session, a virtual connection, i.e. a virtual circuit, is devoted instead.

A particular virtual circuit represents a connection to be made between a particular origination user terminal and a particular destination user terminal. The node switch includes some mechanism to associate the particular virtual circuit with its input and output ports. When information arrives on the input port indicating a virtual circuit, the switch finds the associated output port and makes the desired connection. The connection is maintained only until the information in the packet has traversed the switch to the output port, or until the next packet arrives on the particular input port, typically, whichever is longer. This next packet may indicate another virtual circuit. Then the switch connection is changed to handle this next packet on the input port. Virtual circuits place a greater load on the switching operations that occur at a node, sometimes requiring many millions of switching operations per second.

Before a virtual circuit can be used, as described above, it must be set up in a separate set of transactions. When the communications session is terminated, the virtual circuit must be broken down, also called "taken down" or "torn down" in another set of transactions. Even during the communications session, the virtual circuits have to be maintained, sometimes by changing the connections associated with a virtual circuit in order to accommodate rerouting necessitated by node failure or congestion elsewhere in the network.

With conventional virtual circuits, a separate virtual circuit is set up for each pair of origination user and destination user. The set up transactions include the origination user sending a message to a first node connected to the origination user's terminal. The message requests a connection to the destination user. At the first node, as shown in Figure 4 of the specification, the routing process is executed to determine which of the other nodes connected to the first node should be the next node to get the message requesting the connection. A port linking the first node to the determined next node is identified and stored at the first node with a locally generated virtual circuit identification (VCI), and then the message is forwarded with the VCI to the next node. This process is repeated at all the next nodes, each using locally generated VCIs, until a node is reached that is connected to the terminal of the destination user. If a connection can be established (e.g., the terminal is neither busy nor off) the last node sends an acknowledgment to the preceding node with the VCI sent by the preceding node. Tables or other data structures are updated at the last node to indicate the virtual circuit associated with the VCI. Tables are also updated to indicate that the virtual circuit is established. The preceding node passes the acknowledgment to the next preceding node, identified by the local VCI associated with the VCI in the acknowledgement, until the connection is acknowledged at the first node.

Unfortunately, if two or more nodes are involved in so many communicating sessions that many virtual circuits are needed to carry all the information, one must repeat the laborious set up and tear down process for each of the virtual circuits at each of the intervening nodes. To reduce such repeated operations for essentially the same desired connection between origination node and destination node, permanent virtual circuits have been used. Permanent virtual circuits are those that are set up and remain established for several different communications sessions before being broken down. However, each permanent virtual circuit still must be established individually.

Virtual circuits are named locally by the node that requests them and can be represented by an ID selected from a small set of identifiers. The concept of a virtual path was promoted as part of the Asynchronous Transfer Mode (ATM) protocol to use the same name throughout the network for the same virtual circuit. A virtual path can contain up to 2^{16} (65,536) virtual circuits to uniquely identify all the virtual circuits in a network. Thus a virtual group of VCs can be included in a path. However, 16 bits are needed to specify the virtual circuit within the virtual path. These 16 bits require hardware changes in the switches at the nodes.

The techniques of the present invention allow virtual circuits to be set up and broken down in fewer switch operations than conventional virtual circuits by processing (e.g., setting up, breaking down, and maintaining) a group of virtual circuits together in a virtual circuit bunch (VCB) that does not require the additional hardware of virtual circuit paths. The various characteristics of a VCB are described in the specification. A VCB "establishes a plurality of virtual circuits from one node to at least one other node . . . in response to a single request" (specification, page 4, lines 22-25). "[A] group of virtual circuits [is] pre-established in a virtual circuit bunch" (VCB) (specification, page 23, lines 19-20). As described in the specification "a hierarchy of aliases . . . [is] utilized to conveniently refer to portions of . . . a virtual circuit bunch," (specification, page 23, lines 17-20).

The advantage of such an arrangement is that "Virtual Circuit Bunches [are] utilized to set-up and manage, together, groups of virtual circuits in a flexible way which results in increased performance as well as overcoming the problems of the prior art." (Specification, page 4, lines 5-8.) The virtual circuit bunch (VCB) "enables groups of virtual circuits to be established . . . without any changes to switch hardware" (specification, page 4, lines 10-13).

As an example of the advantages of a VCB, consider the set up of a VCB for communications between node 1 and nodes 3, 4 and 5 described in the specification starting on page 19 with reference

to Figure 7C. In this example, an ATM network is used in which nodes conventionally maintain tables for each input port that associates a local virtual circuit ID (VCI) with an output port, and other tables for each output port that associates a VCI with an input port. The tables and processing are different when a virtual circuit bunch (VCB) is used.

According to this example of the present invention, a packet arrives requesting set up of a VCB. The packet includes an identification of several destinations, specifically, node 4, node 5 and node 3. For each destination, the packet indicates a number of virtual circuits needed, specifically, 8, 8 and 9, respectively, and indicates a level of service needed. The packet of Figure 7C is a single request message that is used to generate 25 virtual circuits from switch 1 to switches 3, 4 and 5. This request message is received at node 2 and is used by node 2 to set up 25 bi-directional virtual circuits (called VCB 3) with node 1.

Assuming that node 2 is physically linked with nodes 3, 4 and 5, then node 2 makes table entries that associate 8 virtual circuits (called VCB 3A) of the 25 virtual circuits VCB 3 with the ports to links going to node 4. Likewise, node 2 makes table entries that associate 8 other virtual circuits (called VCB 3B) of the VCB 3 virtual circuits with ports to links going to node 5. Finally, node 2 makes table entries that associate 9 virtual circuits (called VCB 3C) of the VCB 3 virtual circuits with ports to links going to node 3. Node 2 does all this based on the single request of Figure 7C. Then node 2 sends a single request message to node 4 requesting 8 virtual circuits in VCB 3A. Node 2 sends a similar request to node 5 and another to node 3. Thus four requests are sent during the establishment of this VCB. Using conventional virtual circuits, 50 requests would be needed, 25 requests to node 2, 8 requests to node 4, 8 more requests to node 5 and 9 more requests to node 3.

Node 2 then receives three acknowledgement messages, one each from nodes 4, 5 and 3, respectively. Then node 2 sends a single acknowledgement message to node 1 indicating all 25 virtual

circuits in the request have been established. Using conventional virtual circuits, 50 acknowledgements would be needed, 25 acknowledgments from node 2, 8 acknowledgment from node 4, 8 more acknowledgment from node 5 and 9 more acknowledgment from node 3. Counting both request and acknowledgement messages, a VCB is set up with 6 messages where conventional virtual circuits require 100 messages. This represents a tremendous performance advantage. Note that, the six messages of this example are generated in response to a single request (the first message) to set up the VCB sent by node 1.

Note also that only the 25 needed virtual circuits are specified in the requests. Thus any short name or code that can distinguish 25 different virtual circuits can be used as a name or alias for these virtual circuits. Four bits are sufficient to distinguish up to 32 different items (i.e., 0 to 31, inclusive). There is no need to use a 16-bit naming convention for the virtual circuits in the bunch and thus no need for the hardware additions required for "virtual circuit paths."

After setup, whenever a communications session is needed between a first user at node 1 with a second user at one of the destinations of the VCB, say node 5, then node 2 uses its tables to associate the arriving data message, which specifies destination node 5, with one of the virtual circuits in VCB 3B that is not already being used. Then the control point at node 2 makes an entry into a table of virtual circuits being used by a given input port, sets the switch to connect to the associated output port, and sends the data message on to node 5. The repeated setup and breakdown of individual virtual circuits is eliminated without resorting to virtual circuit paths and the additional hardware that they require.

Other aspects of the invention deal with breaking down virtual circuit bunches, refreshing them, sharing them for fast connect services, split routing of a virtual circuit bunch, interleaving conflicts, and aggregating virtual circuits into existing virtual circuit bunches, among other techniques.

ISSUES

The issues on appeal are:

Whether the Examiner erred in rejecting claims 1, 2, 6, 8, 18, 25 and 29 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne et al., U.S. Patent 5,793,766 (Dieudonne) in view of Fisk, U.S. Patent 5,274,643 (Fisk) and Nishihara et al., U.S. Patent 5,469,543 (Nishihara).

Whether the Examiner erred in rejecting claims 3 and 20 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Hiller et al., U.S. Patent 5,345,445 (Hiller).

Whether the Examiner erred in rejecting claims 7 and 19 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Subramanian et al., U.S. Patent 5,519,707 (Subramanian).

Whether the Examiner erred in rejecting claim 9 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Suzuki, U.S. Patent 4,884,263 (Suzuki).

Whether the Examiner erred in rejecting claims 10, 21-23 and 27 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian.

Whether the Examiner erred in rejecting claims 11-13, 16-17, 26 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller.

Whether the Examiner erred in rejecting claims 14-15, 24, 26, 28 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian further in view of Hiller and furthermore in view of Fisk.

Whether the Examiner erred in rejecting claims 24 and 28 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Fisk.

GROUPING OF CLAIMS

All claims are argued separately, and each claim stands or falls independently of any other claim; except, claim 2 stands or falls with claim 1, claim 7 stands or falls with claim 6, and claim 19 stands or falls with claim 18.

THE ARGUMENT

The Examiner erred in rejecting claims 1, 2, 6, 8, 18, 25 and 29 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara.

Claim 1 recites a "controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." As is clear from the specification, and explained in the summary of the invention above, a virtual circuit bunch (VCB) is different from a group of virtual circuits, and is different from permanent virtual circuits, and is different from a virtual path. One characteristic of a virtual circuit bunch is that all the virtual circuits in the bunch are established as a result of a single request to set up the bunch. Another characteristic of a VCB is that all the virtual circuits in the VCB can be identified with few enough bits that additional hardware changes in a switch are not required. Appellant respectfully submits that the Examiner has only pointed in the references to one of these things that a VCB is not. Thus, the Examiner has not shown where a VCB is taught or suggested in the references.

Dieudonne is directed to multiplexing information from a plurality of sources into a stream of asynchronous transfer mode (ATM) cells (packets) using "the same logical channel." (Dieudonne, Abstract.) Appellants respectfully submit that the logical channel of Dieudonne is just a virtual circuit known in the prior art and described in Appellants' specification. This is not changed by having, in the cell header, a two part name for the logical circuit, the name including a "virtual circuit group

identifier" and a "virtual circuit identifier." The virtual circuit group identifier appears to be just the virtual path identifier known in the prior art. There is nothing in Dieudonne that suggests the logical channel being used is one of a group set up in response to a single request as in a virtual circuit bunch (VCB). There is nothing in Dieudonne that suggests any other characteristics of a VCB. Thus Dieudonne does not teach or suggest the VCB of Appellants' invention. The Examiner admits that Dieudonne does not teach "a group of virtual circuits . . . as a virtual circuit bunch" (December 23, 1999 Office Action, page 2).

The Examiner then relies on Fisk to teach this limitation, citing a passage which states "group virtual circuits to virtual paths" (Fisk, Figure 3). However, as made clear in the specification, a virtual path is not a VCB; therefore the virtual paths of Fisk do not teach or suggest a VCB. There is no reason why one of ordinary skill in the art would conclude that the virtual paths of Fisk differ from the virtual path concept of the ATM protocol that requires additional hardware. For example, Fisk notes that "telecommunication equipment changes . . . In particular telecommunication manufacturer StrataCom . . . has developed network communication modules . . . that groups . . . "virtual circuits" having like characteristics [into] virtual paths" (Fisk, column 1, lines 50-57).

There is nothing in Fisk that shows the virtual paths have any of the characteristics of a VCB. Fisk does not teach how the virtual paths are set up or maintained or broken down. In fact Fisk is not even related to the details of actual, real-time establishment and use of virtual circuits. Instead Fisk is directed to simulating overall network performance in order to design network topology, i.e., the number and connections of nodes in the network. For example, Fisk states that it is an object of the Fisk invention "to provide a network design tool which takes into account the routing of virtual circuits over virtual paths" and "to provide a cost measure" (Fisk, column 2, lines 15-19). Appellants submit that Fisk assumes virtual paths are known, and uses the known properties of virtual paths in a network

design tool. Fisk does not even suggest that virtual paths differ from those known and described in the specification of Appellants' application.

Furthermore the combination is not proper because the Examiner has not given a proper motivation to make the combination. The Examiner suggests one of ordinary skill would modify the switching node of Dieudonne with the virtual path of Fisk "to minimize bandwidth consumption." Fisk is directed to designing a network and Dieudonne is directed to packing information into cells on a single channel, such as a virtual circuit. The Dieudonne network already exists and does not require or make use of the design methods of Fisk. Dieudonne does not profess a need to know what is going on simultaneously in other virtual circuits. The virtual paths modeled by the design tool of Fisk "increase the capacity of the node from 256 to 1024 virtual circuits" but are not shown to affect the amount of data carried by any one virtual circuit. Thus one of ordinary skill in the art reading Dieudonne for improving the carrying capacity of a single virtual circuit would not look to Fisk.

The Examiner cites Nishihara for a controller configured to set up a group of virtual circuits to respective destinations as a virtual circuit bunch. It is respectfully submitted that Nishihara has no disclosure of a virtual circuit bunch. Nishihara teaches level-of-service (LOS) policing circuits in an ATM network to count the number of cells traversing on a given virtual path in order to enforce traffic constraints. Thus, if a virtual path attempts to carry too many packets (cells) in an interval of time, the policing circuit will cut packets that exceed the allotted number, until the next time period begins.

Appellants respectfully submit that there is nothing to suggest that Nishihara is using anything but the prior art virtual path identifier in each cell to associate traffic with a virtual path. Nishihara does not address setting up or breaking down virtual circuits or virtual paths and does not teach or suggest a VCB. For example, Nishihara does not teach or suggest multiple virtual circuits are established in response to a single request. Instead, Nishihara teaches "a VPI (virtual path identifier)

detector 101 for detecting and extracting a VPI from the received cell. The extracted VPI is applied to . . . a VPI-to-SC (service class) translation table 103. . . . A cell counter . . . updates the count value by incrementing the count in response . . ." (Nishihara, column 2, lines 40-49). "[The] translation table 103 produces a service-class identifier . . . and applies it to . . . a SC-to-threshold table 105 . . . [which] converts . . . into a corresponding upper limit value, or . . . 'contract value'," (Nishihara, column 2, line 53, to column 3, line 5). Then if "the count value would exceed the threshold value . . . processor 110 discards the cell" (Nishihara, column 3, lines 13-15). Thus, Nishihara is directed to enforcing level of service (LOS) attributes of a virtual circuit path, and does not even address setting up or breaking down virtual circuits or virtual paths to show any of the characteristics of a VCB, such as setting up all the virtual circuits in response to a single request. Nishihara therefore does not teach a VCB or a controller configured to set up a group of virtual circuits to respective destinations as a VCB.

Because the combination is improper and, in any case, does not reasonably suggest the VCB of claim 1, the rejection of claim 1 under 35 U.S.C. §103(a) is improper. For at least the same reasons, the rejection is improper for claims 2-9 and 20 which depend, directly or indirectly, on claim 1. Thus the rejection is improper for claims 1, 2, 6 and 8.

In addition, claim 6 recites "one of a plurality of virtual circuits of a virtual circuit bunch" which is not shown by any of the references. Since none of the references show a VCB, none can show a virtual circuit of a VCB and none show assigning digital information to such a virtual circuit of a VCB.

In addition, claim 8 recites "virtual circuits of a virtual circuit bunch going to a single destination . . . routed over different paths" which is not shown by the references. Since none of the references show a VCB, none can show virtual circuits of a VCB being routed differently.

Independent method claim 18 recites "assigning a packet to a virtual circuit of a virtual circuit bunch" which are not shown by the references. None of the references teach or suggest a VCB and thus none can assign a packet to a virtual circuit selected from a VCB. Furthermore, the combination of references is improper for the reasons given above. Because the combination is improper and, in any case, does not reasonably suggest the VCB of claim 18, the rejection of claim 18 under 35 U.S.C. §103(a) is improper. For at least the same reasons, the rejection is improper for claim 19 which depends directly on claim 18. Thus the rejection of claim 18 is improper.

Independent computer program product claim 25 recites "assigning a packet to a virtual circuit of a virtual circuit bunch" which are not shown by the references. None of the references teaches or suggests a VCB and thus none can assign a packet to a virtual circuit selected from a VCB. Furthermore, the combination of references is improper for the reasons given above. Because the combination is improper and, in any case, does not reasonably suggest the VCB of claim 25, the rejection of claim 25 under 35 U.S.C. §103(a) is improper. For at least the same reasons, the rejection is improper for claim 29 which depends directly on claim 25. Thus the rejections of claims 25 and 29 are improper.

In addition, claim 29 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions to assign a packet are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for assigning a packet to a virtual circuit of a VDB, they do not, and can not, show transmitting such instructions.

For the reasons given, it is submitted that the Examiner's rejection of claims 1, 2, 6, 8, 18, 25 and 29 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara is untenable. Accordingly, Appellants respectfully request reversal of the rejection.

The Examiner erred in rejecting claims 3 and 20 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Hiller.

Hiller is directed to allocating data from several telecommunication calls into each cell transmitted over a virtual circuit. Hiller mentions “permanent virtual circuits (PVC),” and “a plurality of . . . PVCs is provisioned”, and “only PVCs which have been activated can carry the signals for telecommunications calls” (Hiller, column 2, lines 18-28). However, this disclosure is not the virtual circuit bunch (VCB) of Appellants’ invention. Therefore Hiller does not cure the deficiencies in Dieudonne, Fisk and Nishihara.

Hiller does not teach how the PVCs are first set up or eventually broken down, or which processors or switches maintain a list of PVCs and their activity. Hiller only states that the “ingress node signals the egress node . . . the identification of the PVC” (Hiller, column 4, lines 21-27). Thus there is no showing that the PVCs of Hiller are not merely the virtual circuits and virtual circuit paths of the prior art, requested the same way, set up in separate request messages, and managed the same way by the network. Hiller does not show that the PVCs are set up by a controller configured to set up a group of virtual circuits as a virtual circuit bunch.

Also, there is only one such group. For example, if all PVCs are full, none are added, and the “system busy” condition occurs (Hiller, column 10, lines 23-26, and Figure 15, item 1216). Because there is only one group, there is no need for names of the group. Thus there is no “hierarchy of aliases . . . utilized to conveniently refer to portions of . . . a virtual circuit bunch,” (specification, page 23, lines 17-20).

Only the source terminal knows how many PVCs have been set up and whether they are all busy or not. Only the source terminal applies the methods of FIGs, 15 and 16 of Hiller, cited by the

Examiner. The switches in the rest of the network are not shown to treat the PVCs as a group. Thus a VCB as that term is defined in Appellants' specification is not taught or suggested by Hiller.

Furthermore it is submitted that the combination is not proper. The Dieudonne network already exists and does not require, or make use of, the design methods of Fisk. Dieudonne does not profess a need to know what is going on simultaneously in other virtual circuits. Hiller does not provide a motivation to combine Fisk with the other references.

Claims 3 and 20 depend on claim 1 which recites "a virtual circuit bunch" and "a controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by Dieudonne or Fisk or Nishihara or Hiller for the reasons given above. Because the combination is improper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 1 would be improper. Since claims 3 and 20 depend on claim 1, the rejection is also improper with respect to claims 3 and 20.

In addition, claim 3 recites "a message . . . specifying one or more destinations and a respective number of virtual circuits" which is not shown by the references. The Examiner has never shown where any of the references teach or suggest where a single message specifies a number of virtual circuits. The conventional systems set up each virtual circuit separately and thus do not specify a number of virtual circuits to be set up together. In addition, because virtual circuits are origination and destination specific, more than one destination is never specified in a single set up message, or any message, in the conventional systems. The Examiner has not shown where "more destinations" in a single message are taught or suggested by any of the references. The Examiner cites a passage in Hiller for "requesting a path" (Hiller, Fig. 15, element 1200). However, this element does not teach that a number of virtual circuits are specified in the requesting message, as required by claim 3, or that more than one

destination can be specified in the same message, as recited in claim 3. Thus the modification suggested by the Examiner does not provide the features or advantages of Appellants' claim.

In addition, claim 20 recites "assign . . . to one of a plurality of virtual circuits of a virtual circuit bunch" which is not shown by the references. None of the references teach or suggest a VCB and thus none can assign digital information to a virtual circuit selected from a VCB. In addition, claim 20 recites "in accordance with a user specified policy" which is not shown in the references. The Examiner cites Hiller (Hiller, Fig. 16, column 11, lines 9-15) for this limitation; however, no mention is made in the cited passage of a user specified policy for assigning a virtual circuit.

For the reasons given, the Examiner's rejection of claims 3 and 20 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Hiller should be reversed. Accordingly, Appellants respectfully request such action.

The Examiner erred in rejecting claims 7 and 19 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Subramanian.

Subramanian is directed to setting up virtual paths between a central management supervisor 202 and each of a set of switches in a network. (Fig. 6). On such a logical star arrangement, virtual circuit identifiers can be named by service type 704 and port ID (Fig. 7B). Subramanian uses permanent virtual paths as known in the prior art, but requests those paths from the central management supervisor 202. Specifically, Submaranian teaches a first "virtual service path [is] established between the first switch and the supervisor. Likewise, a second . . . virtual service path [is] established between the second [switch] and the supervisor" (Subramanian, column 3, lines 47-52). No details on setting up the virtual paths are given, so no suggestion is made that these virtual paths differ from the known prior art paths. Submaranian then teaches that "channel numbers within each service path are preassigned by the supervisor" (Subramanian, column 3, lines 55-56). Thus virtual circuit are

not set up together by the switch controllers themselves in bunches, as in Appellant's invention, but instead are set up in conventional ways by the supervisor. There is no suggestion or teaching that the virtual circuits of a virtual path are set up together in response to a single request as in a VCB.

Thus Subramanian does not teach or suggest VCBs or switches with controllers configured to set up at least one group of virtual circuits as a VSB. Subramanian does not cure the deficiencies in Dieudonne or Nishihara or Fisk.

Furthermore, it is submitted that the combination is not proper. Subramanian does not provide a reason to combine actual real-time switching processes like Dieudonne and Nishihara with a design tool like Fisk having different functions and objects.

Claim 7 depends on claim 1 which recites "a virtual circuit bunch" and "a controller configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by Dieudonne or Fisk or Nishihara or Subramanian for the reasons given above. Because the combination is improper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 1 would be improper. Since claim 7 depends on claim 1, the rejection is also improper with respect to claim 7. Claim 7 also depends on claim 6 which recites "one of a plurality of virtual circuits of a virtual circuit bunch" which is not shown by the references for the reasons given above.

Claim 19 depends on claim 18 which recites "a virtual circuit bunch" which is not taught or suggested by Dieudonne or Fisk or Nishihara or Subramanian for the reasons given above. Because the combination is improper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 18 would be improper. Since claim 19 depends on claim 18, the rejection is also improper with respect to claim 19.

For the reasons given, it is submitted that the Examiner's rejection of claims 7 and 19 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Subramanian is not sustainable. Accordingly, Appellants respectfully request reversal of the rejection.

The Examiner erred in rejecting claim 9 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Suzuki.

Suzuki is directed to packet switching in which two or more logical channels are set up for a connection. "In the event of an abnormal condition in the first logical channel the message packets are re-routed to the second logical channel." (Suzuki, Abstract.) Suzuki teaches that the multiple logical channels are set up "in response to each call-setup control packet" and "[a]t the end of a call, all the virtual circuits are released by a call-clearing control packet" (Suzuki, column 3, lines 24-32).

Appellants respectfully submit that Suzuki does not cure the deficiencies in the other references because Suzuki does not teach or suggest a VCB. The attributes of the Suzuki invention do not teach or suggest several characteristics of a VCB. For example, Suzuki does not allow the multiple virtual circuits to go to different destinations. Also, Suzuki does not teach that the multiple logical circuits be pre-established before an individual call or persist beyond the duration of an individual call, as with a VCB. In fact, Suzuki teaches the opposite, that the multiple logical channels should be released upon completion of the call. Therefore, Suzuki does not teach or suggest a VCB.

Furthermore the combination is not proper. Suzuki does not provide a reason to combine actual real-time switching processes like Dieudonne and Nishihara with a design tool like Fisk having different functions and objects.

Claim 9 depends on claim 1 which recites "a virtual circuit bunch" which is not taught or suggested by either Dieudonne or Fisk or Nishihara or Suzuki for the reasons given above. Because the combination is improper, and, in any case, does not teach or suggest every limitation of Appellants'

claim, a rejection of claim 1 would be improper. Since claim 9 depends on claim 1, the rejection is also improper with respect to claim 9.

In addition, claim 9 recites "retransmit" and "cell interleaving problem" which are not shown by the references. Suzuki mentions "heavy traffic" and "trouble" in the passages cited by the Examiner (Suzuki, column 1, lines 33-37), but does not specify "cell interleaving" as the trouble. Also, in the passages cited, the system described must "send a new call-setup packet again to reestablish a new virtual circuit" which teaches away from retransmitting the information to an existing virtual circuit in the VCB.

For the reasons given, the Examiner's rejection of claim 9 under 35 U.S.C. §103(a) as being unpatentable over Dieudonne in view of Fisk and Nishihara and Suzuki is not tenable. Accordingly, Appellants respectfully request reversal of rejection.

The Examiner erred in rejecting claims 10, 21-23 and 27 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian.

Independent claim 10 recites "a virtual circuit bunch" and "a single request . . . to establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian for the reasons given above.

Because the combination does not teach or suggest every limitation of Appellants' claim, a rejection of claim 10 is improper.

Independent system claim 21 recites "a virtual circuit bunch" and "controllers . . . configured to set up at least one group of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian for the reasons given above. Because the combination

does not teach or suggest every limitation of Appellants' claim, a rejection of claim 21 is improper. Since claim 22 depends on claim 21, the rejection is also improper with respect to claim 22

In addition, claim 22 recites "virtual circuit . . . is connected . . . using . . . said virtual circuit bunch" which are not shown by the references for the reasons given above.

The Examiner rejects claim 23 for the same reasons as set forth in claim 21, and rejects claim 27 for the same reason as set forth for claim 23 (Office Action of December 23, 1999, page 12).

Independent computer program product claim 23 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian for the reasons given above. Therefore a rejection of claim 23 under 35 U.S.C. §103 is improper. Claim 27 depends on claim 23, and is allowable for at least the same reason.

In addition, claim 27 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for establishing a plurality of virtual circuits as a VDB, they do not, and can not, show transmitting such instructions.

For the reasons given, it is submitted that the Examiner's rejection of claims 10, 21-23 and 27 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian is not tenable. Accordingly, Appellants respectfully request reversal of the rejection.

The Examiner erred in rejecting claims 11-13, 16-17, 26 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller.

Independent method claim 11 recites "a virtual circuit bunch" and "establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki

or Subramanian or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Appellants' claim, a rejection of claim 11 is improper. Since claims 12-13 and 16 depend on claim 11, the rejection is also improper with respect to claims 12-13 and 16.

In addition, claim 12 recites "setting up switching tables when at least one subsequent node has acknowledged." This is not taught or suggested by the references as the Examiner admits (Office Action of December 23, 1999, page 8). The Examiner argues that a switching table is updated when an acknowledgement is received, but the Examiner does not show where a plurality of "tables" can be set up upon the receipt of "one" acknowledgement from a node, as required by claim 11.

In addition, claim 13 recites "said request . . . specifies a plurality of destinations" which are not shown by the references. Nowhere do the reference disclose a virtual path with virtual circuits going to different destinations. The Examiner points to a passage in Hiller which recites "receive path request" (Hiller, Fig. 15, item 1200). The cited passage does not disclose a single request for a path that specifies a plurality of destinations. A conventional virtual path includes separate virtual circuits that share the same destination (e.g., Hiller, column 2, lines 34-36). When such a path is requested, plural destinations can not be specified. Making such a modification would change the principal of operation of the Hiller invention.

In addition, claim 16 recites "using at least one virtual circuit of said virtual circuit bunch" which is not shown by the references since none of them teach or suggest a VCB.

Independent method claim 17 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller for the reasons given above. Because the combination does not teach or suggest every limitation of Appellants' claim, a rejection of claim 17 is improper.

Independent computer program product claim 26 recites "multicast" and "a virtual circuit bunch" which are not taught or suggested by the references. Neither Suzuki nor Subramanian nor

Hiller teach a VCB for the reasons given above. Furthermore, the Examiner does not show or even address where the references teach a multicast, or allocating a virtual circuit to all nodes participating in a multicast. Therefore a rejection of claim 26 under 35 U.S.C. §103 is improper. Claim 30 depends on claim 26, and is allowable for at least the same reason.

In addition, claim 30 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for allocating a virtual circuit in a multicast using a VDB, they do not, and can not, show transmitting such instructions.

For the reasons given, it is submitted that the Examiner's rejection of claims 11-13, 16-17, 26 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Hiller is untenable. Accordingly, Appellants respectfully request reversal of the rejection.

The Examiner erred in rejecting claims 14-15, 24, 26, 28 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian further in view of Hiller and furthermore in view of Fisk.

It is submitted that this combination is not proper. There is no reason to combine actual real-time switching processes like Suzuki, Subramanian and Hiller with a design tool like Fisk having different functions and objects.

Claims 14 and 15 depend on claim 11 which recites "a virtual circuit bunch" and "establish a plurality of virtual circuits . . . as a virtual circuit bunch." Neither limitation is taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. Because the combination is not proper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a

rejection of claim 11 is improper. Since claims 14-15 depend on claim 11, the rejection is also improper with respect to claims 14-15.

In addition, claim 14 recites "request specifies the number of virtual circuits to be established to each destination" which is not taught by the combination of references. Fisk does not even deal with real time requests. The Examiner has never shown where any of the references teach or suggest where a single message specifies a number of virtual circuits. The conventional systems set up each virtual circuit separately and thus don't specify a number of virtual circuits to be set up together.

In addition claim 15 recites "request specifies the level of service to be provided by one or more virtual circuits." Fisk does not even deal with real time requests. The Examiner has never shown where any of the references teach or suggest where a single message specifies more than one virtual circuit. The conventional systems set up each virtual circuit separately and thus don't specify a number of virtual circuits to be set up together, and therefore can't specify "one or more" virtual circuits.

Independent claim 24 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. In addition, claim 24 recites "aggregating . . . virtual circuits into a virtual circuit bunch" which is not shown by the references. Furthermore, there is no reason to combine actual real-time switching processes like Suzuki, Subramanian and Hiller with a design tool like Fisk having different functions and objects. Because the combination is not proper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 24 is improper.

Independent claim 26 recites "a virtual circuit bunch" and "multicast" which are not taught or suggested by either Suzuki or Subramanian or Hiller or Fisk for the reasons given above. Furthermore, there is no reason to combine actual real-time switching processes like Suzuki, Subramanian and Hiller with a design tool like Fisk having different functions and objects. Because the combination is not

proper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 26 is improper.

The Office Action appealed from rejects claim 28 for the same reasons as set forth in claim 24, and rejects claim 30 for the same reason as set forth for claim 26 (page 13).

Claim 28 depends on claim 24, and is allowable for at least the reasons claim 24 is allowable, given above. In addition, claim 28 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for aggregating a virtual circuit in a VDB, they do not, and can not, show transmitting such instructions.

Claim 30 depends on claim 26, and is allowable for at least the reasons claim 26 is allowable, given above. In addition, claim 30 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for allocating a virtual circuit in a multicast using a VDB, they do not, and can not, show transmitting such instructions

For the reasons given, it is submitted that the Examiner's rejection of claims 14-15, 24, 26, 28 and 30 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian further in view of Hiller and furthermore in view of Fisk is untenable. Accordingly, Appellants respectfully request reversal of the rejection.

The Examiner erred in rejecting claims 24 and 28 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Fisk.

Independent claim 24 recites "a virtual circuit bunch" which is not taught or suggested by either Suzuki or Subramanian or Fisk for the reasons given above. In addition, claim 24 recites "aggregating . . . virtual circuits into a virtual circuit bunch" which is not shown by the references. Furthermore, there is no reason to combine actual real-time switching processes like Suzuk and Subramanian with a design tool like Fisk having different functions and objects. Because the combination is not proper, and, in any case, does not teach or suggest every limitation of Appellants' claim, a rejection of claim 24 is improper.

Claim 28 depends on claim 24, and is allowable for at least the reasons claim 24 is allowable, given above. In addition, claim 28 recites "transmitting said instructions . . . to a destination over a communications interface" which is not shown in the references. The Examiner does not address whether the references show instructions are transmitted to a destination over a communications interface. Furthermore, since the references do not show instructions for aggregating a virtual circuit in a VDB, they do not, and can not, show transmitting such instructions.

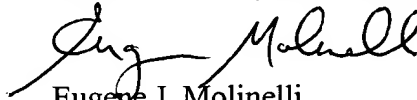
For the reasons given, it is submitted that the Examiner's rejection of claims 24 and 28 under 35 U.S.C. §103(a) as being unpatentable over Suzuki in view of Subramanian and further in view of Fisk is improper. Accordingly, Appellants respectfully request such rejection be reversed.

CONCLUSION

The Examiner has failed to show that that the independent claims are unpatentable over the cited references and failed to make a prima facie case of obviousness against the dependent claims. Each of the claims contains limitations not shown or fairly suggested by the prior art, and each achieves benefits not found in the prior art. Accordingly, Appellant respectfully requests that the Board of Patent Appeals and Interferences reverse the Examiner's rejections.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

A handwritten signature in dark ink, appearing to read "Eugene J. Molinelli", is written over the printed name.

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APPENDIX

- ✓1. A switching node, comprising:
 - a. a switching matrix, and
 - b. a controller to control said switching matrix, said controller configured to set up at least one group of virtual circuits to respective one or more destinations as a virtual circuit bunch.
- ✓2. The switching node of claim 1 in which said switching node is an ATM switch.
- ✓3. The switching node of claim 1 in which said controller sets up a virtual circuit bunch by sending a message to another controller specifying one or more destinations and a respective number of virtual circuits to go to each destination.
- ✓4. The switching node of claim 1 in which said controller keeps all virtual circuits of a virtual circuit bunch to a single destination alive by sending or receiving a refresh packet on less than all of the virtual circuits going to said single destination.
- ✓5. The switching node of claim 4 in which a single refresh packet is used to keep all virtual circuits of a virtual circuit bunch to a single destination alive.
- ✓6. The switching node of claim 1 in which said controller is configured to assign digital information from a source to one of a plurality of virtual circuits of a virtual circuit bunch.

7. The switching node of claim 6 in which the assignment of digital information from a source to one of a plurality of virtual circuits of a virtual circuit bunch is done without assigning said one of a plurality of virtual circuits to a connection.

8. The switching node of claim 1 in which the virtual circuits of a virtual circuit bunch going to a single destination may be routed over different paths.

9. The switching node of claim 1 in which the controller is configured to retransmit digital data from an assigned virtual circuit identifier (VCI) to an alternative VCI of the same or different port going to the same destination when a cell interleaving problem occurs.

10. Computer apparatus for connection to a switching node comprising:

- a. a bus;
- b. an input device, connected to said bus;
- c. a communications interface connected to said bus;
- d. a processor, connected to said bus, said processor configured to receive an input from a user over said input device and to generate a single request to said switching node to establish a plurality of virtual circuits to respective one or more destinations as a virtual circuit bunch.

11. In a digital switching network having a plurality of interconnected nodes, a method of allocating virtual circuits, comprising the step of:

- a. providing an element for performing the step of establishing a plurality of virtual circuits from one node to at least one other node as a virtual circuit bunch in response to a single request.

12. The method of claim 11, in which the step of establishing a plurality of virtual circuits from one node to at least one other node as a virtual circuit bunch includes setting up switching tables when at least one subsequent node has acknowledged the request.

13. The method of claim 11, in which said request specifies a plurality of destinations.

14. The method of claim 13, in which said request also specifies the number of virtual circuits to be established to each destination.

15. The method of claim 11, in which the request specifies the level of service to be provided by one or more virtual circuits.

16. The method of claim 11, further comprising the step of establishing an end to end virtual circuit using at least one virtual circuit of said virtual circuit bunch.

17. A method of allocating virtual circuits in a switching system, comprising the steps of:

- a. identifying virtual circuits at a node going to a common destination node; and
- b. aggregating those virtual circuits into a virtual circuit bunch.

18. A method of providing a fast connect service in a digital switching network, comprising the step of:

- a. assigning a packet to a virtual circuit of a virtual circuit bunch.

19. The method of claim 18 in which a packet is assigned a VCI without setting up a connection.

20. The switching node of claim 1 in which said controller is configured to assign digital information from a source to one of a plurality of virtual circuits of a virtual circuit bunch in accordance with a user specified policy.

21. A system for the transmission of digital communications, comprising:

- a. a plurality of user communication devices;
- b. a plurality of at least partially interconnected switching nodes, each node serviced by a node controller, servicing said user communications devices;
- c. in which at least one of said node controllers is configured to set up a group of virtual circuits to respective one or more destinations as a virtual circuit bunch.

22. The system of claim 21 in which a virtual circuit from a user at one node is connected to a user at a destination node using a virtual circuit from said virtual circuit bunch.

23. A computer program product, comprising:

- a. a memory medium, and
- b. a computer program stored on said memory medium, said computer program comprising instructions for establishing a plurality of virtual circuits from one node to at least one other node of a switching network as a virtual circuit bunch.

✓24. A computer program product, comprising:

a. a memory medium, and

b. a computer program stored on said memory medium, said computer program comprising instructions for identifying virtual circuits at a node going to a common destination node; and for aggregating those virtual circuits into a virtual circuit bunch.

✓25. A computer program product, comprising:

a. a memory medium, and

b. a computer program stored on said memory medium, said computer program comprising instructions for assigning a packet to a virtual circuit of a virtual circuit bunch.

✓26. A computer program product, comprising:

a. a memory medium, and

b. a computer program stored on said memory medium, said computer program comprising instructions for allocating a virtual circuit to all nodes participating in a multicast using a virtual circuit bunch.

✓27. A method of transferring the computer program of claim 23, comprising the step of transmitting said instructions from said memory medium to a destination over a communications interface.

✓28. A method of transferring the computer program of claim 24, comprising the step of transmitting said instructions from said memory medium to a destination over a communications interface.

✓29. A method of transferring the computer program of claim 25, comprising the step of transmitting said instructions from said memory medium to a destination over a communications interface.

✓30. A method of transferring the computer program of claim 26, comprising the step of transmitting said instructions from said memory medium to a destination over a communications interface.